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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,431	04/02/2007	Haruo Suenaga	NGB-41339	8733

52054 7590 12/27/2011

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EXAMINER	
TRAN, THIEN S	

ART UNIT	PAPER NUMBER
3742	

NOTIFICATION DATE	DELIVERY MODE
12/27/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/599,431	SUENAGA ET AL.	
	Examiner	Art Unit	
	THIEN S. TRAN	3742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,5-9,13,14 and 32-38* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,5-9,13,14 and 32-38* is/are rejected.

8)☐ Claim(s) *34* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 34 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 5-9, 13, 14 and 32-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites "rectified voltage / rectified current" in lines 33-34, which the examiner considers as indefinite because it is unclear what is meant by "/". Does the forward slash mean “rectified voltage and rectified current" or “rectified voltage or rectified current”. For examining purposes, the examiner considers "/” to mean or. Appropriate correction is required.

5. Claim 5-9, 13, 14 and 32-38 are also rejected because they are dependent on claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Suenaga (JP 2004-030981) and Kamimura (JP 62-66595). An English-language translation has been provided for Suenaga (JP 2004-030981) and Kamimura (JP 62-66595) and is included in PTO-892 Notice of Reference Cited.

9. Regarding claim 1, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37,

Col 7, Lines 60-63), the series circuit being connected in parallel to the DC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) having to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 35), which are connected to one another, one end of the resonance circuit being connected to a middle point of the series circuit (Fig 1, Item 34 is connected between Items 36 and 37) while the other end of the resonance circuit is connected to one end of the DC power supply (Fig 1, Item 34 is connected to positive terminal of Item 31); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices alternatively or drives the semiconductor switching devices so as to provide a period in which the semiconductor switching devices are turned off concurrently (See Fig 4); a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) that generates a dead time control signal for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

10. Bessyo discloses the claimed invention except for an error signal generation circuit generating an error signal based on a difference between an input current of the

AC power supply and the reference current; and a frequency-modulated signal generation circuit that outputs to the dead time generation circuit a frequency-modulated signal obtained by controlling an amplitude of a rectified voltage / rectified current signal output from the DC power supply based on the error signal, the drive unit limits the lowest frequency of a frequency with the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter.

11. In analogous art of power control method and device for high-frequency dielectric heating, Suenaga discloses an error signal generation circuit (Fig 1, Item 92, 0015 & 0016) generating an error signal based on a difference between an input current of the AC power supply and the reference current (Pg 7, 0011); and a frequency-modulated signal generation circuit (Fig 1, Item 82, 0016 & 0017) that outputs to the dead time generation circuit (Fig 1, Item 39, 0016) a frequency-modulated signal obtained by controlling an amplitude of a rectified voltage / rectified current signal output from the DC power supply based on the error signal (0015 & 0016) for the purpose of providing a power control method for high-frequency dielectric heating free from an influence from the variation of the magnetron or from the temperature variation of an anode of the magnetron (Abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the magnetron control circuit structure of Bessyo with the error signal generation and frequency-modulated signal generation circuit of Suenaga for the purpose of providing

a power control method for high-frequency dielectric heating free from an influence from the variation of the magnetron or from the temperature variation of an anode of the magnetron.

12. The examiner considers the limitations "the drive unit limits the lowest frequency of a frequency with the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter", as functional or intended use language. Claim 1 is directed to a high frequency heating apparatus, and because Bessyo in view of Suenaga discloses all the structure limitations of the claim and is capable of performing the recited function, it meets all the limitations of the claim.

13. While intended use recitations and other types of functional language cannot be entirely disregarded. However, in apparatus, article, and composition claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967); In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963).

14. Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). See also MPEP § 2114.

15. The manner of operating the device does not differentiate an apparatus claim from the prior art. A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

16. Furthermore, In analogous art of control method of magnetron inverter power source, Kamimura discloses the drive unit (Figs 1 & 4d, Item 10f, Pg 16, 18-22), limits the lowest frequency of a frequency with the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter (Pg 4, Lines 6-14) for the purpose of suppressing a voltage current surge cause by a transient phenomenon generated when said inverter and said magnetron start to operate (Pg 4, Lines 6-14). It would have been obvious to one having ordinary skill in the art at the time of the invention to have the drive unit of Bessyo perform the function of limiting the lowest frequency of a frequency with the semiconductor switching devices are driven, so that the lowest frequency is set to be high at the beginning of operation of the high frequency heating apparatus, and the lowest frequency is set to be lower gradually thereafter for the purpose of suppressing a voltage current surge cause by a transient phenomenon generated when said inverter and said magnetron start to operate.

17. Regarding claim 6, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

18. Regarding claim 13, Bessyo teaches the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 36 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

19. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Suenaga (JP 2004-030981) and Kamimura (JP 62-66595) as applied to claim 1, in view of Teruya (Japan Patent Publication 2003-257604). An English-language equivalent has been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and is included in PTO-892 Notice of Reference Cited.

20. Regarding claim 7, Bessyo, Suenaga and Kamimura discloses the claimed invention except for the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been

obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

21. Regarding claim 9, Bessyo, Suenaga and Kamimura disclosed the claimed invention except for the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

22. Claims 8 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Suenaga (JP 2004-030981), Kamimura (JP 62-66595) and Teruya (Japan Patent Publication 2003-257604) as applied to claims 1 and 7, in view of Manabu (Japan Patent Publication 2003-259643).

23. Regarding claim 8, Bessyo, Suenaga, Kamimura and Teruya discloses the claimed invention except for the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga, Kamimura and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

24. Regarding claim 35, Bessyo, Suenaga and Kamimura discloses the claimed invention except for the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency.

25. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the

disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

26. In analogous art of current resonance type soft switching power circuit, Manabu discloses the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga, Kamimura and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

27. Regarding claim 36, Bessyo teaches said a value of the predetermined frequency is variable. Examiner interprets that the predetermined frequency of Bessyo is variable because it is initially set at about 30 kHz and then if the system of Bessyo is turned off, the frequency changes to zero (Col 12, Lines 57-64, operating frequency is 30 kHz and is then lowered & Col 14, Lines 1-12). The frequency is therefore variable because it changes from 30 kHz to 0 khz.

28. Regarding claim 37, Bessyo, Suenaga and Kamimura discloses the claimed invention except for said dead time forming circuit increases the dead time in a step wise manner in connection with an increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses said variable dead time forming circuit increases

the dead time in a stepwise manner in response to a increase in the switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

29. Claims 14 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US 6,362,463), Suenaga (JP 2004-030981) and Kamimura (JP 62-66595) as applied to claim 1, in view of Yang (US 2005/0174819).

30. Regarding claim 14, Bessyo teaches the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning flowing at a predetermined frequency at beginning (Fig 13, Col 13, Lines 50-59) and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo, Suenaga and Kamimura discloses the claimed invention except for the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty

control power supply respectively, and a dead time is generated based on the set of upper and lower potentials.

31. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the set of upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

32. Regarding claim 38, Bessyo teaches input power or an input current control operation is performed by changing at least one of said voltage of the duty control power supply and said switching frequency (Col 9, Lines 8-18).

33. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Suenaga (JP 2004-030981) and Kamimura (JP 62-66595) as applied to claim 1, in view of Manabu (Japan Patent Publication 2003-259643).

34. Regarding claim 32, Bessyo teaches the drive unit (Fig 1, Item 38, Col 8, Line 20) drives the semiconductor switching devices (Fig 1, Items 36 & 37). Bessyo, Suenaga and Kamimura discloses the claimed invention except for further comprising: another series circuit including two semiconductor devices, each of the series circuit and the another series circuit being connected in parallel to the DC power supply, the other end of the resonance circuit is connected to the one end of the DC power supply through a middle point of the another series circuit; and the drive unit drives the semiconductor switching devices of the another series circuit alternatively or drives the semiconductor switching devices of the another series circuit so as to provide a period in which the semiconductor switching devices of the another series circuit are turned off concurrently.

35. In analogous art of current resonance type soft switching power circuit, Manabu discloses further comprising: another series circuit including two semiconductor devices (Drawings 1-3, 5 & 6, Items Q1 & Q1 are set 1, and Items Q3 & Q4 are set 2, Pg 20, Description of Notations), each of the series circuit and the another series circuit being connected in parallel to the DC power supply (Drawings 1-3, 5 & 6, Set 1 [Q1 & Q2] and Set 2 [Q3 & Q4] are in parallel with item E, Pg 20, Description of Notations), the other end of the resonance circuit (Drawings 1-3, 5 & 6, Item 2, Rectification Circuit is connected between Q1 & Q2) is connected to the one end of the DC power supply (Fig 1, Item E, 0019) through a middle point of the another series circuit (Drawing 1, Item 2, Rectification Circuit is connected between Q2 & Q3) for the benefit of providing soft switching in a current resonance type soft switching power circuit (Abstract, Pg 2,

Lines 1-3). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the disclosure of Manabu for the benefit of providing soft switching in a current resonance type soft switching power circuit.

36. The examiner considers the limitations “the drive unit drives the semiconductor switching devices of the another series circuit alternatively or drives the semiconductor switching devices of the another series circuit so as to provide a period in which the semiconductor switching devices of the another series circuit are turned off concurrently" as functional or intended use language. Claim 32 is directed to a high frequency heating apparatus, and because Bessyo, Suenaga, Kamimura and Manabu discloses all the structure limitations of the claim and is capable of performing the recited function, it meets all the limitations of the claim. Paragraphs 10-12 above also apply to claim 32.

37. Regarding claim 33, Bessyo, Suenaga and Kamimura discloses the claimed invention except for further comprising: another series circuit including two capacitors, the series circuit and the another series circuit being connected in parallel to the DC power supply, the other end of the resonance circuit is connected to the one end of the DC power supply through a middle point of the another series circuit.

38. In analogous art of current resonance type soft switching power circuit, Manabu discloses further comprising: another series circuit including two capacitors (Figs 10-12, Items C1a & C1b, 0033), the series circuit and the another series circuit being connected in parallel to the DC power supply (Figs 10-12, Item E), the other end of the

resonance circuit (Figs 10-12, Items 2 & 5, 0033) is connected to the one end of the DC power supply (Figs 10-12, Item E) through a middle point of the another series circuit (Drawings 10-12, Items 2 & 5, Rectification Circuit is connected between Q1 & Q2 and C1a & C1b) for the purpose of forming another half bridge configuration (0033). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga and Kamimura with the another series circuit of Manabu for the purpose of forming another half bridge configuration.

39. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Suenaga (JP 2004-030981), Kamimura (JP 62-66595) and Manabu (Japan Patent Publication 2003-259643) as applied to claims 1 and 32, in view of Noda (US Patent 5,274,208).

40. Regarding claim 5, Bessyo, Suenaga, Kamimura and Manabu discloses the claimed invention except for the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged.

41. In analogous art of high frequency heating apparatus, Noda discloses the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the

capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Suenaga, Kamimura and Manabu with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

Response to Amendment

42. Claims 1, 5 and 6 have been amended.

43. Claims 2-4, 10-12 and 15-31 are cancelled.

44. Claims 32-38 are new.

45. Claims 1, 5-9, 13, 14 and 32-38 are pending.

Response to Arguments

46. Applicant's arguments filed 10/1/2011 with respect to claims 1, 5-9, 13 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

48. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN TRAN whose telephone number is (571)270-7745. The examiner can normally be reached on Mon-Thurs, 8-5PM EST.

50. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Hoang can be reached on 571-272-4780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THIEN S TRAN/
Examiner, Art Unit 3742
12/19/2011

/Henry Yuen/
Supervisory Patent Examiner, Art Unit 3742